R&D

① DTCO(Design-Technology Co-Optimization)

② Bonding

③ Process Integration

Beyond Boundaries
Toward Innovation

DTCO (Design-Technology Co-Optimization)

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About Us

We conduct DTCO (Design Technology Co-Optimization) research at SK hynix, driving product PPA (Power/Performance/Area) improvements through comprehensive optimization of process, device, circuit, and layout, extending to system-level co-optimization.

What We Do

1) Leading comprehensive optimization research for next-generation DRAM platforms, including Stack, PoC, and BSPDN
2) Leveraging various EDA tools to deliver performance predictions and solutions via circuit and system modeling

What We Need to See

Expertise in Semiconductor Engineering, Electrical/Electronic Engineering, Physics, Mathematics, Mechanical Engineering, or a related engineering field, with at least two of the following qualifications:

1) Experience in FinFET-based logic foundry DTCO
2) Proficiency with Synopsys, Cadence, and Ansys tools
3) Experience in system-level product performance simulation
4) Experience in electronic, thermal, and mechanical stress modeling

Ways to Stand Out

1) Experience in circuit design
2) Experience in PDK development for advanced process nodes
3) Programming/Scripting skills in Python, C/C++, or similar languages

Bonding

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About Us

As the Technology Development (TD) team, we drive innovation in next-generation memory technologies. By leveraging wafer bonding capabilities, we develop core process integration technologies to enable new DRAM and NAND architectures and secure a competitive edge in the custom memory market driven by the HBM and AI era.

What We Do

1) Wafer Bonding Process Optimization

Developing core technologies based on hybrid/fusion bonding, and optimizing wafer bonding processes to reduce bonding pitch while ensuring yield and reliability

2) New Architecture Development

Establishing and validating process integration technologies for new DRAM and NAND architectures and platforms enabled by wafer bonding

3) Process Integration and Technical Problem Solving

Managing process integration across pre- and post-bonding processes (trimming, thinning, BEOL, etc.), and proactively analyzing potential defects to resolve technical challenges

What We Need to See

- Expertise in Semiconductor Engineering, Electrical/Electronic Engineering, Physics, Advanced Materials, or a related engineering field
- 5+ years of relevant experience, with all of the following qualifications:

1) Expertise in (hybrid/fusion) wafer bonding process integration, with the ability to lead technology development
2) Expertise in process integration for new DRAM/NAND architectures and platforms utilizing wafer bonding
3) Understanding of process and chip architectures with the ability to collaborate on bonding-related BEOL integration and packaging technologies
4) Ability to analyze characteristics, identify root causes of physical defects, and resolve technical issues

Ways to Stand Out

- Hands-on experience in developing technologies based on an in-depth understanding of wafer bonding mechanisms
- Experience in successfully optimizing advanced processes, including hybrid bonding pitch scaling
- Experience in wafer bonding-related roles at global semiconductor companies (e.g., Micron, Intel, TSMC)

Process Integration

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About Us

We develop wafer bonding and metal layer process integration technologies to establish and manage NAND tech platforms with competitive cost, quality, and performance, while securing and delivering key enabling technologies in a timely manner.

What We Do

1) Next-Generation NAND Architecture Establishment: Leading device structure/design and full-flow process integration to develop core technologies for product implementation
2) Process Optimization & Yield Improvement: Analyzing interactions among unit processes (e.g., Photo, Etch, Cleaning), establishing optimal process conditions, and validating production readiness
3) Data-Driven Problem Solving: Analyzing in-line/electrical data and conducting reliability evaluations to identify defect mechanisms and propose improvement strategies

What We Need to See

- Expertise in Semiconductor Engineering, Electrical/Electronic Engineering, Physics, Advanced Materials, or a related engineering field
- 5+ years of relevant experience, with all of the following qualifications:

1) **PI / Device:** Expertise in metal, under-metal-layer, and wafer bonding process integration for DRAM/NAND/Logic products
2) **Cross-Functional Collaboration:** Ability to lead core technology development through close and flexible collaboration with relevant teams (Process, Device PI, Layout)
3) **Technical Problem Solving:** Ability to analyze characteristics, identify root causes of physical defects, and resolve technical issues

Ways to Stand Out

Experience in metal layer and wafer bonding process integration for 3D NAND/DRAM/Logic products

Experience in core technology development

Experience utilizing computational methods and AI technologies

HBM&DRAM 개발

① Circuit Design(HBM)
② HBM Digital Design (Front-end)
③ HBM Digital Design (Back-end)
④ HBM Digital Design (RTL Design)
⑤ HBM Digital Design (SoC Design)
⑥ HBM Digital Design (Verification)
⑦ HBM PE

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Circuit Design (HBM)

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About Us

As a key organization leading the enhancement of SK hynix's HBM competitiveness, our team is responsible for designing and analyzing HBM products, developing them on schedule, and maximizing customer value.
We partner with leading global AI customers to drive HBM technology innovation, leveraging the latest circuit design expertise and systematic analysis capabilities to build industry-leading competitiveness.

What We Do

- Designing circuits that meet internal and external specification requirements for DRAM/HBM products.
- Improving design quality and enhancing yield to support mass production during the DRAM/HBM product development phase
- Analyzing characteristics at the wafer, KGSD (Known Good Stack Die), and package assembly stages, and evaluating whether product falls within spec.
- Optimizing performance and ensuring stable operation during product dev. in customer systems to deliver a satisfying customer experience

What We Need to See

Expertise in Engineering
(e.g., Semiconductor/Electrical/Electronic/Physical/Computer Science Engineering)
4+ years of experience with one or more of the following capabilities (Master's/Ph.D studies recognized)
1) DRAM or HBM Architecture review and design
2) Full Custom + Digital Co-Design and PDN analysis
3) Full Custom based Logic Foundry design
4) Understanding various tools/equipment for DRAM/HBM product failure analysis

Ways to Stand Out

1) Extensive experience in DRAM or HBM design-related product development and analysis
2) Experience with HBM mounting system analysis
3) Familiarity with Python, Spotfire, Verilog and Circuit Simulator (Hspice, Csim, PrimeSim, Spectre, etc.)

HBM Digital Design (Front-end)

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About Us

As part of SK hynix's HBM Digital Implementation team, you would oversee both digital front-end and back-end design by leveraging the latest process EDA tools, building an efficient development process to secure next-generation HBM competiveness.

What We Do

【 Implementation (Front-end) 】

We are responsible for the entire implementation flow for digital blocks, including implementation and synthesis of DFT architecture, and STA.

We develop HDPF-based interface IPs, such as PCIe and UCIe, and carry out implementations for various digital designs. Leveraging advanced process nodes and the latest EDA tools, we optimize and deliver competitive, customer-tailored HBM solutions with superior PPAT (Performance, Power, Area, TAT).

What We Need to See

Expertise in Engineering (Semiconductor/Electrical/Electronic)

5+ years of experience in one or more of the following

- Experience in PPAT Improvement for Design Optimization of sub-5nm Advanced Processes
- Experience in HPDF Design Top and Block Implementation flow
- Experience with EDA tools required for implementation, including synthesis, STA, and DFT
- Experience in DFT Implementation and Verification (MBIST, Tessent SSH/SSN, TestMAX)
- Experience in Design Analysis and Environment Improvement with Tcl/Python Script

Ways to Stand Out

- Experience with TSMC 3nm Task Implementation
- Experience with HPDF Top Project Management
- Experience with Tessent SSH/SSN-based DFT Implementation and Verification
- Experience with HBM IP (HBM PHY, TSV PHY, 3D PHY) tasks
- Experience with Global Customer Interface and Collaboration

HBM Digital Design (Back-end)

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About Us

As the team responsible for HBM Digital Implementation at SK hynix, we handle both digital front-end and back-end processes using the latest processes and EDA tools, building efficient development processes to secure competitive advantages for next-generation HBM.

What We Do

【 Implementation (Back-end) 】

We manage Digital Auto Place & Route (P&R) for digital blocks in HBM logic die.

Std. We perform various forms of HBM Digital Implementation for both standard and custom HBM. Following customer requirements, we also carry out the implementation of interface IPs, such as PCIe, UCIe, and CXL. We also handle the DTCO domain, engaging in process improvement and optimization, as well as the latest process research, to develop competitive, customer-tailored HBM solutions optimized for PPAT (Performance, Power, Area, TAT).

What We Need to See

Expertise in Engineering (Semiconductor/Electrical/Electronic)

5+ years of experience with one or more of the following capabilities

- HPDF(Tiled) Top Design or project management
- Top Bus/Async Bridge Implementation development
- 2GHz+ High Speed Digital Design development
- Analog/Digital Mixed Design development and Digital IP transition
- PPAT improvement for design optimization in sub-5nm advanced process
- Design analysis and environment improvement using Tcl/Python Script
- Application and operation of latest technologies using EDA Tool for BE(FC/Innovus) and PDN(RHSC/Voltus)

Ways to Stand Out

- Experience with HBM IP (HBM PHY, TSV PHY, 3D PHY) tasks
- Experience with sub-3nm Nanosheet Technology development
- Experience with CPU/GPU/NPU Implementation development
- Experience with Global Customer Interface and Collaboration

HBM Digital Design (RTL Design)

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About Us

As a key organization driving SK hynix's HBM technology competitiveness and global No. 1 market position, our team is responsible for HBM Base Die Digital Design. As part of our team, you would pioneer digital design that determines HBM performance, such as ultra-high-speed interfaces, low-power design and high-reliability logic, and collaborate with global AI leaders to realize next-generation memory technologies.

What We Do

- Directly communicating with customers on specifying requirements and drafting detailed specifications. Collaborating with relevant teams to define IP functions and execute RTL-based design.
- Reviewing Digital IP requirements and determining architecture through PPA evaluations. Designing and verifying IP with RTL and preparing guides for Physical Design
- Logic/Macro Floorplan, Logical Integration, Function Verification, Physical Design Follow-up, Defining Wafer Test Flow, Verifying and Analyzing Issues with Silicon Chip included in Scope of Design and Verification.

What We Need to See

Expertise in Engineering (Semiconductor/Electrical/Electronic/Physics)

5+ years of experience with one or more of the following capabilities

- High Speed Digital PHY and High Speed IP Design and Analysis
- DRAM Memory Controller Design and Analysis
- DRAM DFT/DFD-related Design and Analysis

Ways to Stand Out

- Experience in leading digital design in Interface/Memory PHY and Analog IP
- Experience in TSV Bit Macro and TSV PHY design
- Experience in Mixed Design development (Full-Custom+Digital Design)
- Experience in designing and leading PI for Asynchronous Bridge using Source Synced method for long-distance, high-bandwidth data transmission

HBM Digital Design (SoC Design)

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About Us

Our team is responsible for researching SK hynix's Custom HBM Base-Die Architecture and designing Full-Chip based on it. Key IPs implemented in CHBM include Host, Chiplet Interface IPs, DRAM Controller/PHY IPs and various Logic and Analog IPs

What We Do

- Developing Digital Logic IP/SoC based on Hardware Description Languages (Verilog, VHDL)
- Full-chip design based on In-house & 3rd party IPs and Subsystems
- Subsystem and full chip design considering chiplet-based physical aspects (package-bump, probe-pad, synthesis, etc.)
- Integration and verification of Chiplet Interface PHY/Link/Protocol IP (e.g., UCIe, OpenHBI, BoW, etc.)
- Off-chip Interface PHY/Link/Transaction IP Integration and verification (PCIe, CXL, USB, MIPI, etc.)
- DRAM Controller/PHY IP Integration and verification (LPDDR, DDR, GDDR, HBM)
- RAS requirement analysis and policies, and development & verification of Hardware IPs or Firmware
- Developing and verifying SoC and Digital Logic Verification environments and Verification IPs
- Developing Test Firmware (ARM, RISC-V, etc.) to operate and validate Full-Chip, Subsystem and IP
- Silicon Chip Level Verification, Validation
- Subsystem and Full-Chip Architecture (Power/Debug/Security/DFT)

What We Need to See

- Expertise in Engineering
  (e.g., Semiconductor/Electrical/Electronic/Physical/Mechanical Engineering)
- Candidates with 5 or more experience, who meet one or more of the following requirements

1) Design and verification of Digital Logic IP or Full-Chip based on HDL
2) Performance, Power, and Area estimation through modeling of developed or planned IP/Systems
3) Off-chip/Chiplet Interface PHY/Link Layer design or IP Integration, validation/evaluation
4) Media Controller (NAND, DRAM) design or IP Integration, validation/evaluation
5) Implementing Security Scenarios (Secure Boot, Trust Zone, Attack Detect) to prevent SoC hacking
6) Designing/verifying/evaluating memory and system level RAS policies
7) System-level Clock/Reset & Power Control Logic design and evaluation
8) Analog IP Integration in SoC and DFT Logic Design
9) Design of On-Chip Interconnector (AMBA Bus, NoC, etc.) based on Full-chip requirements and IP/Subsystem specs
10) Subsystem and FullChip Architecture design

HBM Digital Design (Verification)

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About Us

We are responsible for verifying Analog-Digital Mixed IPs, Digital IPs, and Subsystem/Top Level designs to secure SK Hynix's decisive competitive edge in HBM.

To ensure design integrity throughout the HBM product development process, our team handles the entire design verification, which includes building verification systems and environments, along with developing verification models.

What We Do

HBM Digital Design Verification

1) Design verification of In-house, 3rd Party IPs and Mixed signal designs within HBM
2) Developing in-house VIPs for verification and integrating and utilizing third-party VIPs
3) Developing UVM-based verification environments and test cases
4) Achieving code/functional coverage closure through regression testing

What We Need to See

Expertise in Engineering (e.g., Semiconductor/Electrical/Electronic/Computer Science Engineering) with 4+ years of experience in the semiconductor industry (Master's/Ph.D studies recognized), with the following capabilities

1) SystemVerilog/UVM VIP, Testbench and Test Case Development
2) Establishing verification plans and understanding verification processes based on Digital IP Spec.
3) Designing and implementing UVM Agents for new protocols or custom IPs
4) Code/Functional Coverage Closure

Ways to Stand Out

1) Experience in end-to-end (A-to-Z) development of custom UVM Agents based on Spec.
2) HBM, DDR/LPDDR Memory verification
3) Full-Chip Mixed-Level Design (Schematic & RTL) verification

HBM PE

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About Us

We oversee the entire backend process for HBM product development, spanning product engineering (wafer- and package-level testing), customer system-in-package (SiP) validation, and customer support. As we expand into custom HBM solutions, we also lead logic test activities.

What We Do

Developing new test solutions to enhance the quality and productivity of wafer- and package-level test processes for next-generation HBM products, including defect analysis and screening method development

What We Need to See

Master's degree with 5+ years of relevant experience, or a Ph.D., in Semiconductor Engineering, Electrical/Electronic Engineering, Computer Engineering, or a related field, with the following qualifications:

(1) Ability to develop test solutions to overcome ATE limitations
(2) Experience in BOST/test chip development and DFT development, including BIST
(3) Experience in building ATE infrastructure to improve test quality and productivity
(4) Knowledge of DRAM characterization and defect analysis
(5) Knowledge of overall DRAM processes and design

Ways to Stand Out

- Strong understanding of software and hardware
- Experience in or understanding of HBM product development
- Experience in or understanding of DRAM product development
- Strong expertise in ATE
- Proficiency in foreign languages for customer communication

Next Memory Strategy

Beyond Boundaries
Toward Innovation

Next Memory Strategy

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About Us

We drive new business opportunities by analyzing customer pain points and proposing customized memory solutions, while formulating strategies to support executive decision-making.

What We Do

1) Identifying customer pain points by analyzing their business landscape, technologies, and strategies, and formulating customized strategies from a memory perspective
2) Generating new memory business opportunities by analyzing technological trends in AI applications, hardware, and software
3) Developing execution strategies for the AI Infra division, addressing both internal and external initiatives

What We Need to See

5+ years of relevant experience, with **at least three of the following qualificatior**

- Expertise in data center workloads, hardware, and software
- Degree in IT-related fields or equivalent knowledge
- Experience in strategic planning and consulting
- Understanding of the semiconductor industry with experience in analyzing future technology trends
- Experience in AI development or related fields

Ways to Stand Out

- Experience in the Data Center or IT industry
- Experience in strategic planning and consulting
- Experience in technology/market analysis within the industrial sector
- Fluency in English, Chinese or other relevant languages
- Deep understanding of LLM technologies, including Transformer architecture, Prompt Engineering, RAG, and Vector DB

Infra Tech.

① Materials Technology(EDTW)

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Toward Innovation

Material Technology (EDTW)

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About Us

We develop etch gases, deposition gases, precursors, and targets, along with wafer materials, for semiconductor etch, diffusion, and thin film processes. Aligned with our technology roadmap, we ensure timely delivery of high-performance core materials to breakthrough critical process challenges in DRAM, NAND, and next-generation memory.

What We Do

【Ion/Radical Etching Mechanism Design & Passivation Control for New Etch Gases via Plasma Dissociation】

- Optimizing key etch steps grounded in plasma physics and designing gases to reduce process variation and improve yield
- Leading development of 2D Conventional, Metallic, ALE, Cryo, and Low GWP etch gases

What We Need to See

Expertise in Semiconductor Engineering, Electrical/Electronic Engineering, Physics, Advanced Materials, Chemistry, Chemical Engineering, or a related engineering field

5+ years of relevant experience, with all of the following qualifications:

- Expertise in etch gas element chemistry, fragmentation, etch reaction gas design, property prediction, quality control, and chemistry understanding
- Ability to understand the correlation between etch gases and key plasma etch process factors (process recipes, analytical tools, and equipment) to design new etch gases, combined with proficiency in designing customized etch gases and predicting optimal process parameters through TCAD/AI-based approaches
- Comprehensive understanding of etch processes, equipment, and gas materials

Ways to Stand Out

- Experience at material or equipment suppliers in etch gas and process development
- Background as a memory/logic semiconductor etch process engineer or in new etch gas material R&D

SK hynix

CAD Engineering

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Toward Innovation

CAD Engineering

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About Us

Our team plays a key role in strengthening SK hynix's competitive edges of next-generation HBM and memory products by developing and validating design data that defines timing, power, and variation characteristics. Based on advanced process technology and CAD solutions, we develop high-quality design kits and improve design methodologies to drive innovation in next-generation memory technologies.

What We Do

- Developing and maintaining IP Design Kits for the development of next-generation HBM and memory products
- Performing characterization of Std. Cells and Custom IPs to develop Libraries and ensure the quality and consistency of Design Kits used in the design environment
- Managing QoS for Design Kits and developing methodologies for new characterization and design

• Performing characterization of Std. Cells and Custom IPs to develop and verify Libraries
• Managing the quality of IP Design Kits and maintaining integrated database
• Automating characterization and developing new methodologies

What We Need to See

Bachelor's Degree in Engineering (e.g., Semiconductor, Electronic, Physics)
5+ years of experience with the following experience:

- Cell characterization and library development
- SPICE-based circuit analysis and model verification
- Liberty(NLDM, CCS, LVF)-based library creation and quality verification
- Development and maintenance of Design Kit or quality control

Ways to Stand Out

- Experience characterizing Memory, Custom, and Analog IPs
- Experience developing Advanced Node (<5nm) Libraries or Design Kits
- Experience managing large-scale Libraries and Design Kit Database

IR Communication

Beyond Boundaries
Toward Innovation

IR Comm.

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Our Team

As the interface between SK hynix and the capital markets, IR Comm. team communicates the company's performance and strategy to the market with transparency and consistency, while connecting market and investor feedback to management activities. Through data-driven analysis and company-wide collaboration, the team develops IR messages and communications on business performance, industry conditions, and business strategy.

What We Do

【Planning and Executing Strategic IR】 Organizing quarterly earnings release conference calls; developing IR messages based on analyses of financial and non-financial data, global peer trends and valuation; and developing IR strategies and plans in collaboration with management and relevant teams.

【IR Events】 Planning and managing domestic and global IR events including corporate presentations, NDRs, conferences, etc. Preparing related materials.

【Stakeholder Communications】 Regular/ad-hoc communication with domestic and global institutional investors and analysts

【Market·Peer Analysis】 Analyzing stock markets, industries, and peers to derive insights

What We Need to See

4+ years of work experience and all of the following qualifications and competencies:

1. 4 to 8 years of work experience in capital markets (e.g., IB, research, asset management, PE) or IR experience at a listed company in Korea or overseas
2. Research skills to derive insights from data
3. Near-native proficiency in English business communication skills (for English materials preparation and meetings with global investors)

Ways to Stand out

- IR or relevant experience in global companies
- Expertise or work experience in semiconductor manufacturing
- Experience analyzing, categorizing and summarizing reports from securities firms and institutional investors
- Professional certifications in finance/accounting (e.g., CFA, AICPA)