

R&D



**Beyond Boundaries
Toward Innovation**

Modeling

#Icheon #Junior & Expert



About Us

Our organization is responsible for SPICE modeling for AA, with a focus on accurately analyzing the electrical characteristics of semiconductor devices and translating them into models for circuit design applications. Based on a deep understanding of semiconductor processes and device characteristics, we develop highly accurate SPICE models by correlating measurement data with simulation results. We continuously validate and enhance these models to ensure reliable prediction of actual circuit and product behavior.

What We Do

The role involves FinFET, GAA, and RF modeling, with responsibilities including compact model development and parameter extraction. The position focuses on accurately modeling device characteristics to develop highly accurate and reliable SPICE models for circuit design applications. Automation and AI-driven modeling technologies are also leveraged to continuously improve model accuracy and predictive capability

What We Need to See

Expertise in semiconductor, Electronics, Electrical Engineering, Physics, or related field

6+ years of experience with expertise in at least one of the five areas below.

- 1) FinFET /GAA Spice Modeling
- 2) Device RF Modeling
- 3) Parameter Extraction & Model validation
- 4) Circuit-Aware Modeling

Ways to Stand Out

- 1) FinFET SPICE Model Development Experience
- 2) FinFET Device Test Pattern Development & Layout Design Experience
- 3) FinFET, Advanced-Node LDE, RF & Noise Modeling Experience

DRAM & NAND Development

- ① HBM Foundry PI
- ② Product Engineering
- ③ System Analysis – Linux/AI SW
- ④ System Analysis – MC RTL & R/H
- ⑤ Application Engineering
- ⑥ Software
- ⑦ NAND Design_Analog



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HBM Foundry PI

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About Us

Our team plays a key role in driving SK Hynix's HBM technological competitiveness and its position as the global market leader. We develop key enabling technologies for next-generation HBM products and lead HBM implementation through close collaboration with global foundry partners. Additionally, to develop various forms of Customized HBM (CHBM), we partner with design houses, serving as the technical interface for overall outsourced production, thereby realizing future HBM technologies.

What We Do

- 1) Conduct Foundry-Design-Package Linked DFM (Design for Manufacturability) Co-Optimization for HBM logic die development
- 2) Optimize logic die characteristics through Foundry PDK (Process Design Kit) analysis and improvements to design rules and models
- 3) Derive PDK enhancements and operate technical review meetings through collaborative engagement with Foundry partners

What We Need to See

Expertise in Engineering (Semiconductor/Electrical/Electronic/Physics) with one or more of the following capabilities and 5+ years of experience

- 1) Hands on experience with PDK/DFM/Design Rule in Foundry Process or Fabless environment
- 2) Experience with DRC/DRM Tool, such as Calibre, Pegasus or ICV
- 3) (3) Foundry Design and layout capabilities

Ways to Stand Out

- 1) Experience in Advanced Nodes (5nm or below) or EUV processes
- 2) Experience in DRM for Advanced Packaging, such as HBM, Chiplet, 2.5D/3D
- 3) Former Foundry employees with specific experience in Technology Development (TD) or Process Integration (PI)
- 4) Excellent English communication skills to support global collaboration

HBM Product Engineering

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About Us

We oversee the entire back-end process for HBM product development, spanning product engineering (wafer- and package-level testing), customer system-in-package (SiP) validation, and customer support. As we expand into custom HBM solutions, we also lead logic test activities.

What We Do

- Building and managing HBM production test baselines for global SoC customers
- Setting up logic test environments for customer IPs and performing troubleshooting on issues arising during product development.
- Analyzing and optimizing production test results to ensure yield and quality
- Validating the characteristics of logic and memory through wafer/PKG-level silicon tests
- Identifying defect mechanisms to derive corrective actions

What We Need to See

5+ years of work experience in OSAT Test with the following capabilities and experience:

- Experience in Wafer/CoW/WoW Level Silicon Test
- Overall knowledge in logic process and design
- Experience validating characteristics of logic and memory and analyzing defects

Ways to Stand Out

- Experience in test setup for global SoC customers and trouble shooting
- Experience in OSAT
- Experience in optimizing production test baselines

System Analysis – Linux/AI SW

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Our Team

We define the value of DRAM from a holistic system perspective, expanding our focus from hardware to applications. We analyze diverse memory requirements driven by workload changes and offer optimal configurations. Our scope of work ranges from existing systems such as servers, mobiles devices, and GPUs to next-generation DRAM architectures, including CXL memory or PIM.

What We Do

We perform system-level analysis of AI workloads within AI server and data center environments, develop memory solutions and drive productization.

Analyzing AI Workload: Analyzing LLM learning/inference or RAG from the perspective of GPU/xPU system and quantify its impact on memory subsystems

Optimizing AI SW Stack: Identifying and resolving memory bottlenecks across the entire stack from inference frameworks (e.g., vLLM, SGLang) to PyTorch, CUDA runtime, and Kernel

Develop Linux Kernel: Modify and develop Linux Kernel in Memory Management and Driver areas to validate and optimize the performance of new memory solutions

Propose Next-Generation Memory Spec: Deriving new specifications based on analysis results and incorporate them into product development strategy

What We Need to See

Bachelor's Degree in Computer/Electronic Engineering or expertise in related fields (5+ years of work experience)

- 1) Ability to analyze and modify Linux Kernel code with hands-on development experience particularly in Memory Management and Device Driver areas
- 2) Understanding of AI/LLM workload behavior and the architecture of AI SW Stacks
- 3) Strong ability to independently identify problems and develop solutions in advanced technology fields

Ways to Stand Out

- 1) Experience in contributing to Linux Kernel or major open source projects
- 2) Experience in modifying and optimizing architectures of vLLM, SGLang, TensorRT-LLM
- 3) Experience in developing GPU/Accelerator architectures and SW Stacks
- 4) Global communication skills

System Analysis – MC RTL & R/H

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About Us

We define the value of DRAM from a holistic system perspective, expanding our focus from hardware to applications. We analyze diverse memory requirements driven by workload changes and offer optimal configurations. Our scope of work ranges from existing systems such as servers, mobile devices, and GPUs to next-generation DRAM architectures, including CXL memory or PIM.

What We Do

- Co-optimizing memory controller and DRAM for next-generation memory products such as custom HBM and 3D Stacked DRAM
- Developing controller-DRAM integrated simulation models and exploring design space in advance, based on analysis on commercial MC IP and understanding of RTL-level behavior
- Building performance and power prediction models correlated with silicon measurement data and identifying optimal controller-DRAM design solutions before the system is finalized
- Analyzing DRAM security and reliability issues, such as RowHammer, based on silicon measurements and proposing product-optimized protocols and solutions
- Defining memory design strategies based on real workloads through system-level modelling from application, SW stack, xPU, and to DRAM

What We Need to See

Bachelor's Degree in Computer Science and Electronic Engineering or expertise in related fields (5+ years of work experience)

We are looking for candidates with the ability to:

- 1) Understand RTL code behavior and develop performance models based on that.
- 2) Leverage the knowledge of DRAM Security/RowHammer to propose new solutions.
- 3) Understand DRAM operations and DRAM memory controller architectures and analyze the RTL.
- 4) Analyze memory traffic of real-world workloads and assess the impact of DRAM on system performance.

Ways to Stand Out

Candidates with the following experience is preferred:

- 1) Designing, verifying, or optimizing the performance of DRAM Memory Controllers
- 2) Designing SoC memory subsystems and interconnects
- 3) Publishing papers on DRAM RowHammer and demonstrating the technical depth through peer review at relevant conferences (Computer Architecture)
- 4) In-depth knowledge of GPU architectures or simulation of GPU-based systems

Application Engineering

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About Us

Our team overseas the reliability of memory systems. Moving beyond verification, we preemptively eliminate risks that may arise during early development stage through data-driven analysis and ensure system stability with optimal ECC/RAS solutions. In this role, you will serve as a key solution architect, safeguarding product quality and customer trust.

What We Do

This role involves analyzing memory errors arising in servers and customer system environments and developing ECC and RAS solutions to enhance system reliability. Especially, the role requires a deep understanding of Linux Kernel-based memory error reporting and handling mechanisms and the ability to review new error correction algorithms or solutions and explore the feasibility of high-availability architectures that are applicable to next-generation memory technologies.

What We Need to See

Expertise in Computer Science, Electronic Engineering or related fields

(5+ years of work experience)

- 1) In-depth understanding of Linux Kernel internals (especially memory management and EDAC subsystem) and experience in kernel module development and debugging
- 2) Ability to analyze system-level error scenarios and develop solutions (based on expertise in ECC algorithms and RAS architectures)
- 3) Understanding of the roles and responsibilities of a system engineer at SK hynix and the ability to proactively solve problems through close collaboration with customers and internal development teams

Ways to Stand Out

- 1) Experience in the Linux Kernel community or contribution to related patches
- 2) Hands-on experience with system boot, initialization, and error-handling processes on server platforms (e.g., x86, ARM)
- 3) Understanding of server management interfaces and protocols such as BMC, IPMI, or Redfish
- 4) Experience developing system-level firmware and software using C, C++, Python, and etc.
- 5) Global communication skills

Software

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About Us

Our team specializes in developing end-to-end system validation solutions for all memory products. Spanning the entire software stack—from BIOS firmware to OS and application layers—we eliminate potential risks before they arise during system integration. We are enhancing our capabilities through close collaboration with global partners and ensuring system reliability by independently developing and implementing memory validation software optimized for advanced system architectures.

What We Do

- Building memory validation environments within customer system platforms and developing in-house SW solutions
- Analyzing and improving test environments based on customer logs and utility program benchmarking, and interpreting and optimizing firmware-based memory initialization, power-up sequences, and training operations.
- Studying HBM validation environments on GPU platforms and developing in-house SW solutions by using CUDA, OpenCL SDK, etc.

What We Need to See

- 1) Ability to perform system validation and debugging on GPU/NPU platforms by modifying AI workloads and AI SW stacks
- 2) Experience developing GPU computing programs using CUDA or OpenCL SDKs
- 3) Experience with GPU platform-based system validation or GPU diagnostic/validation environments (e.g., NVVS, DCGM)
- 4) Understanding of GPU execution and memory models and ability to design CUDA kernels
- 5) Experience with Linux-based development environments and Python automation scripting

Ways to Stand Out

- 1) Experience analyzing and developing GPU drivers, CUDA Runtime or system SW
- 2) GPU memory(HBM/VRAM) data integrity validation: experience designing CUDA kernel-based pattern tests and stress tests
- 3) GPU system failure analysis: experience analyzing failure mechanisms related to fail addresses, patterns, and temperature dependencies
- 4) Experience using GPU diagnostic tools such as NVVS and DCGM and analyzing coverage

NAND Design-Analog

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About Us

Our team handles the verification of analog circuits essential for NAND operations and the development of new IPs. We also manage power levels and consumption for both internal and external power sources of the NAND device.

What We Do

- Conducting checklist simulations to verify analog IP characteristics, exploring ideas for circuit improvements, and developing new IPs tailored to customer requirements
- Managing internal NAND power circuits and deriving improvement strategies, designing and verifying Power Distribution Networks (PDN) for internal and external sources, and estimating and controlling total power consumption

What We Need to See

Expertise in Engineering (i.e., Semiconductor, Electronic, Electrical, Computer)

2+ years of experience with the following capabilities (No prior work experience is required for Ph.D. holders):

- (1) Knowledge of semiconductor processes, device physics, and analog circuit analysis
- (2) Experience with Schematic & Layout design tools and SPICE-based simulation tools

Ways to Stand Out

- Experience in NAND development and analog circuit design tasks
- Experience in designing analog IPs or power management circuits in the semiconductor industry

Solution Development

- ① SoC Design
- ② SoC Design Verification
- ③ Digital IP Design
- ④ High-Speed Interface



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SoC Design

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About Us

Our team designs controllers that are embedded in NAND solution products. We manage the end-to-end design process, from IP design to SoC integration. Through close collaboration with the Firmware team, we optimize HW-SW interoperability. Additionally, we deliver high-efficiency, low-power, and high-performance controllers through RTL design and architecture research focusing on PPA(Power, Performance, Area).

What We Do

We integrate diverse IPs and subsystems to construct the overall SoC architecture while defining interfaces and designing the high-level RTL. I will also participate in the integration and interface design of PCIe/UCle Controller and PHY IP.

Moreover, we closely work with FW, Verification, PD, and DFT teams to drive successful tape-out of PPA-optimized SoC controllers.

What We Need to See

Expertise in Electrical/Electronic/Semiconductor Engineering or related majors

3+ years of experience in SoC Top-level RTL Design and IP Integration

Experience in designing AMAB(AXI,AC)-based interfaces

Experience in ASIC-based SoC design and tape-out

Experience in partitioning and controlling Clock, Reset, and Power domains

Understanding of Synthesis and Timing

Experience in collaboration with front-end and back-end teams

Problem-solving skills and team-oriented mindset

Ways to Stand Out

Experience in leading full-chip SoC designs including Interfaces, Memory PHYs, and Analog IPs.

Design, integration, and verification experience with PCIe/UCle Controller or PHY IP.

Proficiency in AI tools and English communication skills

SoC Design Verification

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About Us

We are a leading R&D hub developing next-generation SoCs for Controllers for SSDs and mobile devices, as well as AI-oriented storage products. With global top-tier verification frameworks and automation environments, we create semiconductor solutions with maximized performance and power efficiency. We are looking for passionate talents who will join us in pushing the boundaries of technology.

What We Do

We play a critical role in ensuring the functional accuracy and reliability of SoCs.

- Verification Environment Build: Designing and implementing reusable verification environments (Testbench) based on SystemVerilog and UVM.
- Test Strategy Planning: Establishing verification plans through spec analysis and developing test scenarios to achieve target coverage.
- Simulation and Debugging: Identifying bugs proactively through simulation and resolving issues through collaboration with the design teams.
- Sign-off Verification: Analyzing functional and code coverage to ensure all sign-off criteria are met, finalizing the approval for tape-out.
- Process Advancement: Enhancing overall development productivity by developing verification automation scripts and introducing innovative methodologies.

What We Need to See

Expertise in Electrical/Electronic/Semiconductor Engineering or related majors

3+ years of work experience in SoC verification

Problem-solving skills and team-oriented mindset

Ways to Stand Out

Proficiency in AI tools and English communication skills

Digital IP Design

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About Us

Our team is an advanced research organization at SK Hynix leading the R&D of High-Speed Interface IPs essential for a wide range of products, including Chiplet, Mobile, and SSD.

Our key development area include Chiplet D2D IPs, UFS MIPI IPs, TSV PHYs, and NAND PHYs, and we also develop platforms to test these technologies.

Dedicated to our core mission of driving innovative technological breakthroughs, we invite your interest and applications to join our dynamic team.

What We Do

Designing and modeling DSP circuits for High-Speed SerDes PHYs

Experience in developing Analog/Digital Mixed-Signal Processing circuits for MIPI M-PHY and PCIe PHYs

Designing RTL, verifying functions, and analyzing Silicon Chip Validation issues

Key tasks involve executing mixed-signal simulations integrating modeled analog circuits with RTL designs, along with designing and validating DSP RTL circuits

What We Need to See

Bachelor's degree or higher in Engineering (i.e., Semiconductor, Electronics, Electrical, Computer, Physics, Mechanical) with one or more of the following capabilities:

- (1) Ability to design and verify PCIe PHY / M-PHY DSP
- (2) Ability to design and verify Chiplet IPs (e.g., UCle)
- (3) Ability to design and verify Memory Interface of NAND/DRAM

Ways to Stand Out

- (1) Experience in designing IPs, including Interface/Memory PHYs and Digital IPs.
- (2) Experience in developing/verifying Chiplet Interfaces or integrating 3rd-party IPs.
- (3) Experience in developing and leading SoC Platform projects involving ARM Cores and AMBA Bus architectures.
- (4) Experience in Digital Circuit Design and Front-End Implementation.
- (5) Proficiency in AI tools and strong English communication skills are preferred.

High-Speed Interface

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About Us

Our team is a dedicated mixed-signal design organization focused on designing MIPI PHYs, the core of next-generation high-speed interface IPs. We are simultaneously leading the mass production of M-PHY 6.0 and the advanced development of M-PHY 7.0, while defining and implementing ultra-high-speed SerDes architectures based on the latest FinFET processes.

We manage the entire development lifecycle—from architecture design and circuit design to silicon verification—within a single organization. Here, we work in an environment where System, Digital, and Analog engineers collaborate closely. Our mission is to deliver the best-in-class power efficiency and signal integrity demanded by the mobile storage market.

What We Do

- Designing high-speed SerDes circuit architectures compliant with M-PHY 7.0 specifications
- Defining SerDes channel architectures to support increased data transmission speeds and establishing Link Budget and Equalization (EQ) strategies
- Designing DSP-based CDR structures and optimizing Jitter and BER performance
- Designing Full Custom circuits and providing layout guidelines considering FinFET process characteristics
- Verifying system operations including power management domains (AON/PSW) and validating specification compliance through Mixed-Signal simulations

What We Need to See

- Experience in SerDes circuit design and FinFET-based circuit design
- Experience in designing DSP-based CDRs
- Experience in defining and designing high-speed Interface or SerDes architectures
- Knowledge of SerDes and analog circuits
- Master's or Ph.D. in a related field, or equivalent practical experience

Ways to Stand Out

- Experience in developing based on standard high-speed interface specifications such as MIPI M-PHY, PCIe, and USB.
- Experience in designing Equalization circuits (CTLE, DFE, FFE) and channel compensation circuits
- Experience in analyzing, measuring, and debugging Jitter and Signal Integrity
- Experience in mass-production chip development and silicon evaluation
- Experience in Multi-Power Domain architecture and Ultra-Low Power (ULP) design

Materials Technology (Patterning)



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Materials Technology(Patterning)

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About Us

Our team develops photoresist and interlayer materials for semiconductor lithography processes. We overcome the limitations of lithography materials arising from scaling and develop critical materials in a timely manner to address process challenges for next-generation products and transfer them to the process. Through these efforts, we contribute to securing stable lithography process margins and strengthening product competitiveness.

What We Do

【 Developing photoresist materials for Lithography 】

- Designing and developing photoresist materials
- Discovering and evaluating the characteristics of new polymer, PAG, quencher and additive materials
- Analyzing material characteristics such as resolution, sensitivity, and LWR
- Managing product application and quality stabilization
- Developing materials in advance for next-generation chip processes

What We Need to See

Expertise in Engineering (i.e., Chemistry, Chemical Process, Polymer, Materials)

5+ years of experience with the following capabilities:

- Experience in developing Photoresist or semiconductor materials
- Understanding of lithography processes and material mechanisms
- Knowledge of polymer synthesis and organic chemistry
- Data analysis and problem-solving skills

Ways to Stand Out

- 5+ years of experience in the synthesis and development of raw materials for EUV resist
- Experience in the design and research of next-generation materials such as Metal Oxide Resist and Molecular Resist

Safety, Health, Environment



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SHE(Safety)

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About Us

As a global leader and technology innovator in the semiconductor industry, SK hynix places the highest value on people and the environment. Within SK hynix, our team operates a structured safety management system covering more than one million work activities each year. We reduce potential on-site risks at the source and manage safety systems for semiconductor manufacturing equipment and facilities to help prevent safety incidents.

What We Do

- 1) Standardizing safe work standards and enhancing related systems
- 2) Operating consulting and support programs for the work safety management system
- 3) Managing work risk assessment and standard operating procedure systems
- 4) Operating the integrated safety work permit system and enhancing the work permit system
- 5) Conducting incident investigations, accident analysis, and initiatives to reduce similar or recurring incidents
- 6) Managing Safety Common Spec. for semiconductor equipment and facilities and conducting compliance inspections

What We Need to See

Expertise in Safety Engineering, Industrial Safety, Chemical Engineering, Electrical Engineering, or Mechanical Engineering, with the following qualifications:

- 1) 4+ years of experience in safety work permits, work risk assessments, or related work
- 2) Experience in incident investigations, accident analysis, or risk management under the Serious Accidents Punishment Act
- 3) Experience conducting safety assessments for facilities or work safety management systems
- 4) Engineer-level certification or higher in Safety, Chemical Engineering, Gas, or Electrical fields

Ways to Stand Out

- 1) Holder of Professional Engineer Safety or Certified Industrial Safety Consultant license
- 2) 3+ years of safety management experience at a global semiconductor company
- 3) Experience in building and operating safety management system for overseas offices

Safety Management

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About Us

As Korea's leading semiconductor company and a global technology leader, SK hynix places the highest value on people and the environment. Within SK hynix, our team works with company-wide SHE teams to provide tailored safety management for services and facilities managed by Corporate Culture (HR, ER, and ED), helping prevent safety incidents.

What We Do

- 1) Applying safety policies and standards on site
 - Communicating company-wide safety policies and standards and monitoring implementation
 - Supervising work activities and reviewing standard operating procedures and risk assessments
 - Planning and conducting safety theme inspections
- 2) Providing tailored safety management support for corporate services, such as cafeterias, commuting services, dormitories, and other non-FAB areas

What We Need to See

Expertise in Safety Management and Safety Engineering with the following qualifications:

- 1) 3+ years of hands-on safety management experience in employee facilities and workplace infrastructure
- 2) Experience assessing or consulting on safety and health management systems in service operations
- 3) Engineer level certification or higher in Safety, Health, or a related field

Ways to Stand Out

- 1) Strong understanding of corporate services and extensive field experience, in addition to hands-on safety management experience
- 2) Experience managing safety for contractors, vendors, or service providers
- 3) Strong communication skills with service management teams and partner companies
- 4) Strong understanding of semiconductor or chemical manufacturing industries

Growth Strategy



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Global Growth Strategy

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About Us

Amidst the paradigm change in the AI industry, our team discovers new business opportunities to define SK hynix's mid- to long-term growth strategies. We conduct in-depth analysis of global AI industry trends and technology and market shifts to support the executive management's key decision-making. Also, we develop business strategies across the value chain of AI and semiconductors and identify strategic investment opportunities.

What We Do

- 1) **Strategic Problem Solving:** We structure complex business challenges in the AI and semiconductor industries with strategic reasoning and data-driven analysis and develop and propose solutions.
- 2) **Tech-Business Synthesis:** We discover new growth opportunities by translating global AI technology trends and market changes into business narratives and analyze and assess business viability.
- 3) **Market & Tech Intelligence:** We analyze how the global macroeconomic shifts and technology trends of AI and semiconductors impact the semiconductor business and develop response scenarios for risk mitigation.

What We Need to See

- 5 to 10 years of work experience with the following experience or capabilities:
- Deep understanding of the semiconductor and AI industry ecosystems and hands-on experience of analyzing technological trends
 - Strategic business analysis capabilities to assess business viability and develop investment rationale
 - Ability to translate complex technological issues into structured business narratives (storytelling)
 - Excellent communication skills with the ability to collaborate with diverse teams and drive outcomes
 - Proficiency in communicating with diverse stakeholders in a global business environment

Ways to Stand Out

- Experience in strategic consultation or business viability analysis for investment or new business (Prior experience at a strategy consulting firm is preferred.)
- Extensive understanding of the upstream/downstream of semiconductor and AI industries and market intelligence skills
- Global experience (e.g., education, semiconductor-related work experience)

Infra Purchase - Logistics



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Logistics

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About Us

Our team builds and operates logistics systems for company-wide efficient production and operations and improves work process continuously for timely response to internal and external business environment.

What We Do

- Export and import transportation of goods associated with production and sales (equipment, raw materials, (semi-)finished goods, etc.)
- Planning and improving logistics
 - Building operational strategy for logistics and optimizing operations (transportation/insurance contract management, MI)
 - Optimizing logistics networks (building and improving transport routes and hubs)
 - Operating/managing/improving logistics systems and data analysis
 - Analyzing and optimizing logistics costs

What We Need to See

- Experience in export/import logistics management and planning at a manufacturing company or in international export/import transportation at a logistics company
- 2 to 4 years of work experience in related fields

Ways to Stand Out

- Experience in optimizing global logistics of advanced technology products such as semiconductors
- Experience in building and implementing company-wide logistics system
- Holder of certifications in international logistics management